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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,017	01/02/2002	David Arnold Luick	ROC920010189US1	7517

7590 10/13/2005

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EXAMINER	
MAI, TAN V	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,017	LUICK, DAVID ARNOLD	
	Examiner	Art Unit	
	Tan V. Mai	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,18-29 and 31-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33* is/are allowed.

6)☒ Claim(s) *1-7,10-14,18-29,31 and 32* is/are rejected.

7)☒ Claim(s) *8,9 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Applicant's arguments with respect to claims 1-7, 10-14, 18-29, 31 and 32 have been considered but are moot in view of the new ground(s) of rejection.

3. Claims 1-7, 10-14, 18-29, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al (US Pat 5,548,546).

Jang et al (US Pat 5,548,546) have been discussed in paragraph No. 5 (Paper mailed 4/27/05).

The amended independent claims add detail "feature":

> "wherein at least one stage in the pipelined circuit stalls **by one or more clock cycles** in response to the carry out **signal to account for additional delay introduced by incrementing the second result when the carry out signal Indicates a carry**" (claim 1;

similar language is used in other independent claims). It is noted that the actual "feature" is not explicitly shown in Jang et al's Figures; however, such "feature" is implicitly disclosed from the Figures and the corresponding recitation. It is also noted that Jang et al's Fig. 4 broadly show the "conditional incrementer" having AND gates (405-407) and Ex-OR gates (401-404); however, the actual "conditional incrementer" should have memory means (such as buffer or delay elements) and clock feature for

providing substantially simultaneous the desired data to / from the gates. Also, see (1) Patti et al, col. 5, lines 24-32:

> "In the drawings, broad arrows represent busses for conveying multiple-bit parallel digital signals and line arrows represent connections for conveying analog signals or single bit digital signals. Depending on the processing speed of the devices, **compensating delays** may be required in certain of the signal paths. One skilled in the art of digital signal processing circuit design would know where such **delays** would be needed in a particular system"

and (2) Virtue (Figs. 2 and 4-5) shows delays and clock feature between elements. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Jang et al's teachings because the device is a parallel adder having "conditional incrementer" as claimed.

4. Claims 1-7, 10-14, 18-29, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al (US Pat 5,912,833).

Jang et al (US Pat 5,912,833) have been discussed in paragraph No. 5 (Paper mailed 4/27/05, second occurance).

The amended independent claims add detail "feature":

> "wherein at least one stage in the pipelined circuit stalls **by one or more clock cycles** in response to the carry out **signal to account for additional delay introduced by incrementing the second result when the carry out signal Indicates a carry**" (claim 1;

similar language is used in other independent claims). It is noted that the actual "feature" is not explicitly shown in Jang et al's Figure 1,element 13; however, such "feature" is implicitly disclosed from the Figures and the corresponding recitation. However, the actual "conditional incrementer" should have memory means (such as buffer or delay elements) and clock feature for providing substantially simultaneous the desired data to / from the gates. Also, see (1) Patti et al, col. 5, lines 24-32:

> "In the drawings, broad arrows represent busses for conveying multiple-bit parallel digital signals and line arrows represent connections for conveying analog signals or single bit digital signals. Depending on the processing speed of the devices, **compensating delays** may be required in certain of the signal paths. One skilled in the art of digital signal processing circuit design would know where such **delays** would be needed in a particular system"

and (2) Virtue (Figs. 2 and 4-5) shows delays and clock feature between elements. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Jang et al's teachings because the device is a parallel adder having "conditional incrementer" as claimed.

5. Claims 1-7, 10-14, 18-29, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu et al (US Pat 6,832,235).

Muramatsu et al (US Pat 6,832,235) have been discussed in paragraph No. 7 (Paper mailed 4/27/05).

The amended independent claims add detail "feature":

> "wherein at least one stage in the pipelined circuit stalls **by one or more clock cycles** in response to the carry out **signal to account for additional delay introduced by incrementing the second result when the carry out signal Indicates a carry**" (claim 1;

similar language is used in other independent claims). It is noted that Muramatsu et al do NOT specifically detail the claimed "feature"; however, the "feature" is merely a basic component in the electronic device for buffer / store the desire data in the pipelined computation processing. For example, see (1) Patti et al, col. 5, lines 24-32:

> "In the drawings, broad arrows represent busses for conveying multiple-bit parallel digital signals and line arrows represent connections for conveying analog signals or single bit digital signals. Depending on the processing speed of the devices, **compensating delays** may be required in certain of the signal paths. One skilled in the art of digital signal processing circuit design would know where such **delays** would be needed in a particular system"

and (2) Virtue (Figs. 2 and 4-5) shows delays and clock feature between elements. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Muramatsu et al's teachings because the device is a parallel adder having "conditional incrementer" as claimed.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cited references are art of interest.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan V. Mai whose telephone number is (571) 272-3726. The examiner can normally be reached on Mon-Wed and Fri. from 9:30am to 2:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki, can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is:

Official (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Tan V. Mai
Primary Examiner